Segundo Desafio

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**VHDL**

library IEEE;

use IEEE.std\_logic\_1164.all;

entity prior\_detect is

port(

P0, P1, P2, P3 : in bit;

X0, X1, INT : out bit

);

end prior\_detect;

architecture nv\_logic of prior\_detect is

begin

process (P0, P1, P2, P3)

begin

if (P0 = '1') then

X0 <= '0';

X1 <= '0';

INT <= '1';

elsif (P1 = '1') then

X0 <= '1';

X1 <= '0';

INT <= '1';

elsif (P2 = '1') then

X0 <= '0';

X1 <= '1';

INT <= '1';

elsif (P3 = '1') then

X0 <= '1';

X1 <= '1';

INT <= '1';

else

X0 <= '1';

X1 <= '1';

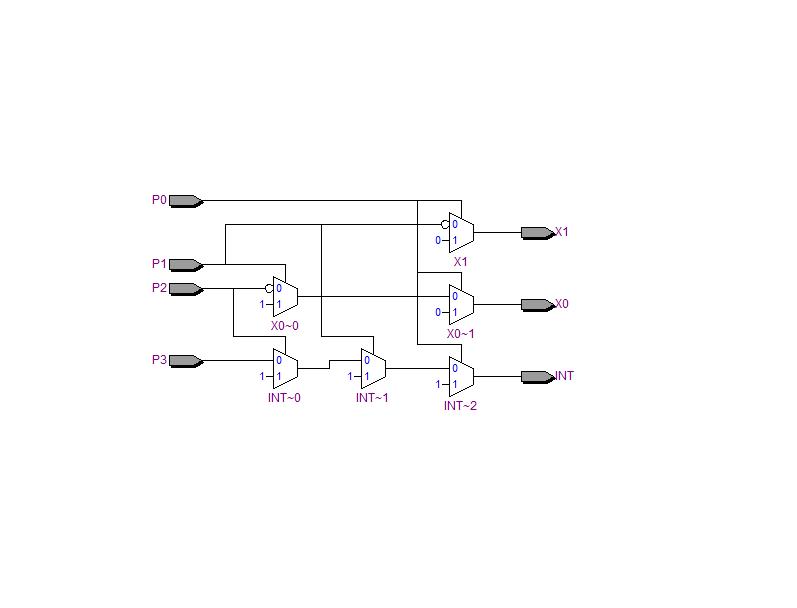
INT <= '0';

end if;

end process;

end nv\_logic;

**RPL**



**Sim waveform**

